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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/606,724 | 06/26/2003 | Billy D. Hart | 02CR168/KE | 5809 |

7590 03/26/2007

ROCKWELL COLLINS, INC.
Attention: Kyle Eppele
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400 Collins Rd. NE
Cedar Rapids, IA 52498

| EXAMINER | |
|---|---|
| BURD, KEVIN MICHAEL | |
| **ART UNIT** | **PAPER NUMBER** |
| 2611 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 03/26/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/606,724 | HART ET AL. | |
| | Examiner | Art Unit | |
| | Kevin M. Burd | 2611 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20* is/are allowed.

6)☐ Claim(s) *1-5,7-16,18 and 19* is/are rejected.

7)☒ Claim(s) *6 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. This office action, in response to the remarks filed 1/12/2007, is a non-final office action.

***Response to Arguments***

2. Applicant's arguments with respect to claims 1-5, 7-16, 18 and 19 have been considered but are moot in view of the new ground of rejection.

3. The previous objection to the drawings has been withdrawn. The claimed limitations are shown in figure 2.

4. A new objection to drawings is stated below.

***Drawings***

5. Figures 4 and 5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Objections***

6. Claim 6 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 20. When two claims in an application are duplicates or else are so close in

content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-5, 7-16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loseke (US 6,449,244) in view of Gray (US 2003/0005008) further in view of Schuurmans ((US 7,079,061).

Regarding claims 1 and 4, Loseke discloses an apparatus for efficiently performing parallel processing of high-speed samples comprising an A/D converter 14 in figure 1 (column 6, lines 16-18). Demux 16 is a serial-to-parallel converter for converting the samples from the A/D 14 into parallel samples. Loseke discloses the demultiplexed data outputs 18 are converted from real to complex data representations (column 6, lines 30-32). The real and complex data representations of the input signal are channelized on individual channels (column 6, lines 46-54). Loseke discloses filtering the parallel signals (figure 1, filter 22). Loseke does not disclose decimating-by-two the parallel signals. Gray discloses a method of providing signal processing operations where each parallel stream is processing signals at a lower rate than the

signal data rate itself while resulting in an overall signal processing rate suitable for high rate signal processing (abstract). Figure 2 describes the filtering of the input signal in parallel paths. The data stream will be split into eight parts for filtering and each part will operate at approximately $1/8^{th}$ the signal-processing rate of the filter of figure 1. This is described in more detail in paragraphs 0020 and 0021. Gray discloses the invention contemplates any number of parallel paths (paragraph 0020). Therefore, when two paths are selected, each path will operate at one half the signal-processing rate. In addition, Gray discloses figure 3 shows the parallel signals being down sampled to 50% the input rate (paragraph 0030). Gray discloses signal processing can be difficult when the signal is a high rate signal (paragraph 0005). Gray states the present invention allows devices with a lower signal processing rate to be used in the parallel processing paths, avoiding many of the problems facing prior art high data rate signal processing (paragraph 0009). For these reasons, it would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of Gray into the apparatus of Loseke. The combination of Loseke and Gray discloses an A/D converter for converting the received analog signal but does not disclose the A/D converter is a 1-bit A/D converter. Schuurmans discloses a sigma delta A/D converter that is a 1-bit A/D converter (column 1, lines 20-35). Schuurmans discloses an advantage of the 1-bit A/D converter is that it has a perfect linearity. In addition the converter is a simple circuit (column 1, lines 20-25) and therefore will reduce the cost and complexity of the circuit. For these reasons, it would have been obvious for one of ordinary skill in the art at the

time of the invention to combine the 1-bit A/D converter of Schuurmans into the apparatus of the combination of Loseke and Gray.

Regarding claim 2, Gray discloses the system performs convolution at a rate of 1/M that of the sample rate (paragraph 0038).

Regarding claims 3, Loseke discloses the real and complex data representations of the input signal are channelized on individual channels (column 6, lines 46-54) from the quadrature mix circuit.

Regarding claim 5, Gray discloses the filter and decimate statges as stated above.

Regarding claims 7 and 10, Loseke discloses a method of implementing an apparatus for efficiently performing parallel processing of high-speed samples comprising an A/D converter 14 in figure 1 (column 6, lines 16-18). Demux 16 is a serial-to-parallel converter for converting the samples from the A/D 14 into parallel samples. Loseke discloses the demultiplexed data outputs 18 are converted from real to complex data representations (column 6, lines 30-32). The real and complex data representations of the input signal are channelized on individual channels (column 6, lines 46-54). Loseke discloses filtering the parallel signals (figure 1, filter 22). Loseke does not disclose decimating-by-two the parallel signals. Gray discloses a method of providing signal processing operations where each parallel stream is processing signals at a lower rate than the signal data rate itself while resulting in an overall signal processing rate suitable for high rate signal processing (abstract). Figure 2 describes the filtering of the input signal in parallel paths. The data stream will be split into eight

parts for filtering and each part will operate at approximately 1/8$^{th}$ the signal-processing rate of the filter of figure 1. This is described in more detail in paragraphs 0020 and 0021. Gray discloses the invention contemplates any number of parallel paths (paragraph 0020). Therefore, when two paths are selected, each path will operate at one half the signal-processing rate. In addition, Gray discloses figure 3 shows the parallel signals being down sampled to 50% the input rate (paragraph 0030). Gray discloses signal processing can be difficult when the signal is a high rate signal (paragraph 0005). Gray states the present invention allows devices with a lower signal processing rate to be used in the parallel processing paths, avoiding many of the problems facing prior art high data rate signal processing (paragraph 0009). For these reasons, it would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of Gray into the apparatus of Loseke. The combination of Loseke and Gray discloses an A/D converter for converting the received analog signal but does not disclose the A/D converter is a 1-bit A/D converter. Schuurmans discloses a sigma delta A/D converter that is a 1-bit A/D converter (column 1, lines 20-35). Schuurmans discloses an advantage of the 1-bit A/D converter is that it has a perfect linearity. In addition the converter is a simple circuit (column 1, lines 20-25) and therefore will reduce the cost and complexity of the circuit. For these reasons, it would have been obvious for one of ordinary skill in the art at the time of the invention to combine the 1-bit A/D converter of Schuurmans into the apparatus of the combination of Loseke and Gray.

Regarding claim 8, Gray discloses the system performs convolution at a rate of 1/M that of the sample rate (paragraph 0038).

Regarding claim 9, Loseke discloses the real and complex data representations of the input signal are channelized on individual channels (column 6, lines 46-54) from the quadrature mix circuit.

Regarding claim 11, Gray discloses the filter and decimate statges as stated above.

Regarding claims 12, 15, 18 and 19, Loseke discloses an apparatus for efficiently performing parallel processing of high-speed samples comprising an A/D converter 14 in figure 1 (column 6, lines 16-18). Demux 16 is a serial-to-parallel converter for converting the samples from the A/D 14 into parallel samples. Loseke discloses the demultiplexed data outputs 18 are converted from real to complex data representations (column 6, lines 30-32). The real and complex data representations of the input signal are channelized on individual channels (column 6, lines 46-54). Loseke discloses filtering the parallel signals (figure 1, filter 22). Loseke does not disclose decimating-by-two the parallel signals. Gray discloses a method of providing signal processing operations where each parallel stream is processing signals at a lower rate than the signal data rate itself while resulting in an overall signal processing rate suitable for high rate signal processing (abstract). Figure 2 describes the filtering of the input signal in parallel paths. The data stream will be split into eight parts for filtering and each part will operate at approximately $1/8^{th}$ the signal-processing rate of the filter of figure 1. This is described in more detail in paragraphs 0020 and 0021. Gray discloses the invention

contemplates any number of parallel paths (paragraph 0020). Therefore, when two paths are selected, each path will operate at one half the signal-processing rate. In addition, Gray discloses figure 3 shows the parallel signals being down sampled to 50% the input rate (paragraph 0030). Gray discloses signal processing can be difficult when the signal is a high rate signal (paragraph 0005). Gray states the present invention allows devices with a lower signal processing rate to be used in the parallel processing paths, avoiding many of the problems facing prior art high data rate signal processing (paragraph 0009). For these reasons, it would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of Gray into the apparatus of Loseke. The combination of Loseke and Gray discloses an A/D converter for converting the received analog signal but does not disclose the A/D converter is a 1-bit A/D converter. Schuurmans discloses a sigma delta A/D converter that is a 1-bit A/D converter (column 1, lines 20-35). Schuurmans discloses an advantage of the 1-bit A/D converter is that it has a perfect linearity. In addition the converter is a simple circuit (column 1, lines 20-25) and therefore will reduce the cost and complexity of the circuit. For these reasons, it would have been obvious for one of ordinary skill in the art at the time of the invention to combine the 1-bit A/D converter of Schuurmans into the apparatus of the combination of Loseke and Gray.

Regarding claims 13 and 14, Loseke discloses the real and complex data representations of the input signal are channelized on individual channels (column 6, lines 46-54) from the quadrature mix circuit.

Regarding claim 16, Gray discloses the filter and decimate stages as stated above.

### *Allowable Subject Matter*

Claim 20 is allowed.

Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Burd whose telephone number is (571) 272-3008. The examiner can normally be reached on Monday - Friday 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kevin M. Burd
3/21/2007

KEVIN BURD
PRIMARY EXAMINER